Designing Transmission Lines and Line Drivers
Chapter 13

Introduction to Secure Transmission Lines[1]

The intent in a secure environment is to reduce or prevent sensitive signals from escaping the controlled area through either common-mode coupling paths into the ground and/or power system, or by radiating to the outside world. While shielding and controlled access might work as a bulk approach, and although opto-isolators work to reduce common-mode coupling, in the majority of cases networks and systems are simply built as needed, with security controls applied as they become necessary.

One of the greatest sources of system generated emissions escaping a security controlled medium is through cable radiation associated with improperly terminated transmission lines. Regardless of whether the cable is short, such as between a keyboard and a pc, or long, such as a hardwired twisted pair network, wires are never matched at all frequencies, and some level of reflected signals and associated standing waves nearly always exists. This chapter examines primarily interface circuits, focusing on transmission line theory, interface cabling, and transceiver interface design. The goal of this discussion will be to provide guidance for the system designer in reducing the potential for leakage of secure emissions as a result of improper line driver/receiver designs, while at the same time maintaining interface signal specifications.

Transmission Line Theory

Systems are connected to one another via transmission lines. There are three interface components making up the standard hardwired transmission system, the line driver, the transmission line itself, and the line receiver. The transmission line is usually a single wire, coaxial cable, parallel wire, or twisted pair. Signals are transmitted over the interface using single ended or differential techniques as shown in Figure 13-1.

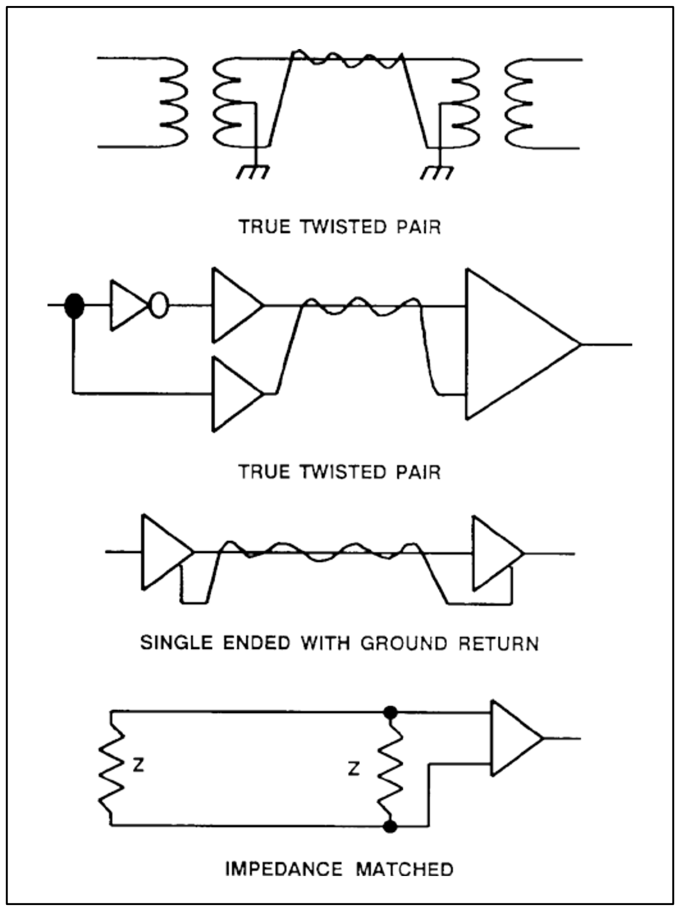

Figure 13-1 Transmission Line Techniques

[1] NOTE: This chapter does nor repeat what is incorporated in the Text*: Hard Wire and Cable Design in Secure Communications,* written by this author.

Looking at a forward traveling wave on an interface transmission line, the voltage can be represented at the input as:

$$V_{D=0} = \Re V_f e^{(j\omega t)}$$

where f represents the forward direction, and D represents location. The corresponding forward traveling wave at a later time and position can be represented as

$$V_D = \Re V_f e^{j\omega(t-[\frac{D_f}{v_{(0)}}])}$$

where $v_{(0)}$ is the velocity of the wave, and ω is the radian frequency. Similarly, a backward (b) traveling wave at position D can be represented as:

$$V_D = \Re V \, e_b^{j\omega(t+\frac{D_b}{v_{(0)}}]}$$

Combining equations (2) and (3) gives an expression for a conductor with two traveling waves moving in opposite directions:

$$V_D = \Re e^{j\omega t}\,[V_f e^{-j\omega\{\frac{D_f}{v_{(0)}}\}} + V_b e^{j\omega\{\frac{D_b}{v_{(0)}}\}}]$$

Calculating the corresponding current at position D gives the following expression:

$$I_D = \Re \frac{e^{j\omega t}}{z}\,[V_f e^{-j\omega\{\frac{D_f}{v_{(0)}}\}} - V_b e^{j\omega\{\frac{D_b}{v_{(0)}}\}}]$$

$$V_D = V_f e^{-jBD_f} + V_b e^{jBD_b}$$

Here z is the impedance of the conductor (at position O). The negative sign is due to a backward propagating wave, while current, by convention, always flows in the forward direction. Equations (4) and (5) show the variation of voltage and current with time and with distance along the line. The real part of ejωt is cos ωt. If the rms value of either the voltage or current is considered instead of the instantaneous values and if a phase constant is defined as B = ω/υ, then the above equations can be simplified as follows:

$$I = \frac{1}{Z(0)}\,[V_f e^{-jBD_f} - V_b e^{jBD_b}]$$

The equations above represent the variation of the rms values with distance along the line. These variations are called standing waves.

The input impedance of the transmission line can be derived from the equations above if the input boundary is defined at -l, or z = -l. The l (= l) in the equation is the same as D above.

$$Z_{(-1)} = z_{(0)} \left[\frac{e^{-jBl} + \rho\, e^{jBl}}{e^{-jBl} - \rho\, e^{jBl}} \right]$$

The reflection coefficient, ρ, is an important parameter in the understanding of power transfer. That is, the reflection governs the transfer of voltage and current from the sending end to the receiving end of a transmission line. The reflection coefficient of a load (L) impedance when given a characteristic impedance for the line can be found from:

$$\rho = \frac{Z_L \;\; z_o}{Z_L + z_o}$$

where z_0 is the characteristic impedance and Z_L is the load or terminating impedance.

It is relatively easy to see that if the cables are infinitely long, or if they are terminated in their characteristic impedance, then $Z_{(L)} = z_{(O)}$, and ρ goes to zero.

Going back to the expression for input impedance (equation (8), the equation can be written in terms of the reflected wave from load end $Z_{(2)}$ in the sine cosine form as:

$$Z_{(1)} = z_{(0)} \left[\frac{Z_{(2)} \cos Bl + jz_{(0)} \sin Bl}{z_{(0)} \cos Bl + jZ_{(2)} \sin Bl} \right]$$

Formula (10) is absolutely correct. However, if the numerator and denominator are both divided by cos Bl, the equation again reduces to a simpler form:

$$Z_{(1)} = z_o \left[\frac{Z_2 + jz_o \tan Bl}{z_o + jZ_2 \tan Bl} \right]$$

A second useful expression for describing the transmission line characteristics is the voltage standing wave ratio. If the two traveling waves from equation (8.6) are examined closely, it appears that the first term becomes more negative while the second term becomes more positive in phase as $z_{(O)}$ increases. At some value $z_{(O)}$, the two terms will be in phase and the voltages in the forward (f) and backward (b) direction will add, giving a maximum voltage. At a distance of one quarter wavelength, the voltages will be out of phase and will subtract, giving a minimum voltage.

$$V_{SWR} = \frac{V_{(\max)}}{V_{(\min)}} = \frac{V_{(f)} + V_{(b)}}{V_{(f)} - V_{(b)}}$$

The voltage standing wave ratio can now be defined in terms of the absolute (pos) values of the maximum and minimum voltage values as:

$$V_{SWR} = \frac{1 + \rho}{1 - \rho}$$

The reflection coefficient is defined as ρ = V(b)/V(f), and is always less than 1 except for open or short lines. Therefore, the voltage standing wave ratio can be written in terms of the reflection coefficient in the following equation.

Notice what the previous analysis implies to a TEMPEST designer. Specifically, the reflection coefficient increases with impedance mismatch, and a large coefficient implies a large VSWR.

While large standing waves might not create a problem for normal data transfer, the resultant radiated emissions create the potential for TEMPEST compromises over a very large bandwidth. One way to reduce the standing waves is through impedance matching, but this is impossible for all frequencies of interest. Therefore, let's take a look at cable and line driver/receiver parameters to discover if some simple solutions to Red line interface problems are achievable.

Cable Characteristics

The resistive component of a transmission line over a short distance is relatively small when compared to the input impedance of the line receiver in a typical application. Distributed capacitance, however, will combine with the resistive component to produce a RC time constant that degrades the waveform of the digital transmitted signal. The higher the capacitance or the longer the transmission line, the more the signal is rounded off or otherwise degraded. Cable line capacitance per foot is a good indication of the usefulness of the transmission line to individual applications, and is generally available in the cable manufacturer's specifications.

In addition to cable capacitance, other restrictions on cable line length include signal bit rate, duty cycle, bit width, and receiver sensitivity. The maximum bit rate per length of transmission wire is a function of the bit width and duty cycle of the data stream. For the line driver and receiver combination of Figure 13.2, the maximum bit rate that can be transmitted over 100 feet of Belden #8795 twisted pair cable {z(o) = 100 ohms, C = 15 pf/ft, propagation delay = 1.3 msec/ft) at a 10 % or 90 % duty cycle is approximately 7.5 Mb/sec, whereas the maximum bit rate for a 50 % duty cycle is approximately 37 Mb/sec. The 5:1 ratio between 10 % and 50 %

duty cycles is reflected in the 5:1 ratio in the curves of Figure 13-2. Additionally, the required signal bandwidth is approximately equal to the inverse of the bit width, which is determined from the data rate and duty cycle of the transmitted signal.

What is immediately apparent from the above information is that commercial system or network transmission line cabling is produced for maximum rather than minimum data transfers. In other words, there is sufficient capacity in standard interface cabling that a significant amount of additional capacitive and resistive loading can be added to a relatively short transmission line before the intended data transfer is interfered with. By carefully evaluating the proposed line driver characteristics, a good idea of how much loading to add can be determined.

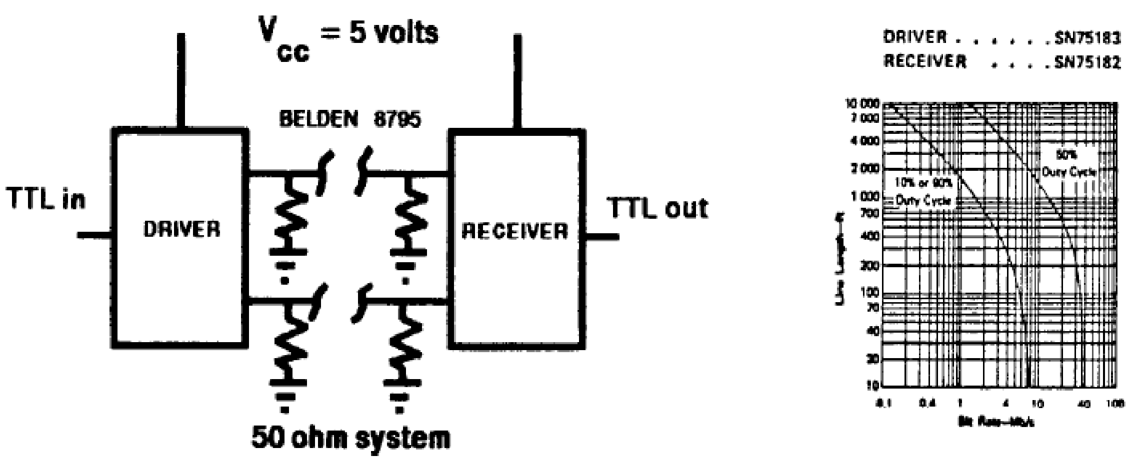

Figure 13- 2 Curves for Line Driver & Receiver Combination (Belden 8795 Cable)

Line Driver Characteristics and Wave Shaping

Important line driver characteristics are output impedance, output peak current capability, and frequency response. The output peak current capability and frequency response can be obtained from the manufacturer's specifications. To reduce reflections, the driver's output impedance should equal the characteristic impedance of the transmission line with the receiver attached.

Not only should the impedance match at the intended frequency, but significant impedance matching or line damping should continue to the higher frequency range where square wave harmonics can cause transmission line reflections. This could mean the addition of variable impedance loads such as ferrites or capacitor banks.

For the design Engineer, the line driver's circuitry is most important because that is where wave shaping techniques are employed. Wave shaping at the driver involves controlling and smoothing the signal rise time, which, in effect, decreases the reflection produced at the impedance mismatch, and controls the amount of signal crosstalk to adjacent lines. Again, it is important to note that resultant standard output waveforms must conform to the applicable interface specification levels such as those listed in EIA Standard RS-423-A (see Figure 13-3).

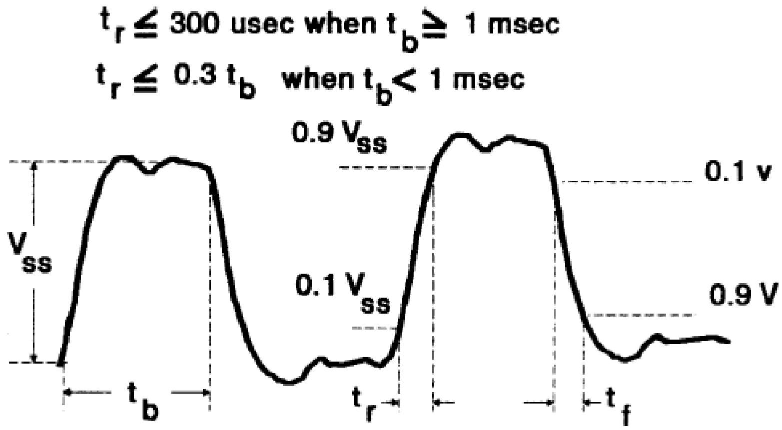

Figure 13-3 EIA Standard RS-423-A Wave Shaping

While significant flexibility for wave shaping is provided by this specification, some special applications, such as those specifically intended to enhance TEMPEST emission control, do not necessarily need to conform to the standard specification. Most importantly, dedicated secure systems can usually conform to whatever is necessary for them to be operable.

There are two types of wave shaping, linear and exponential. Linear wave shaping is used for rise times of 100 usec or more, while exponential is used for faster rise times. Both linear and exponential can be accomplished directly on many standard line drivers, and can also be accomplished using DIP RC filters. DIP type RC filters will be discussed following the section on practical line driver/receiver designs.

Considering direct wave shaping on the driving device, Texas Instrument's uA9636AC is a dual line driver with adjustable slew-rate (wave shaping input) for both RS-232-C and RS-423 applications. The wave shaping control is provided to both the line drivers through one input pin. For linear wave shaping, a resistor is connected between the wave shaping control pin and ground which can control the output to almost straight line rise and fall times.

For exponential wave shaping, a series resistor and capacitor (Figure 13-4) are normally connected between the control pin and ground with the resultant RC time constant tuned to the desired response.

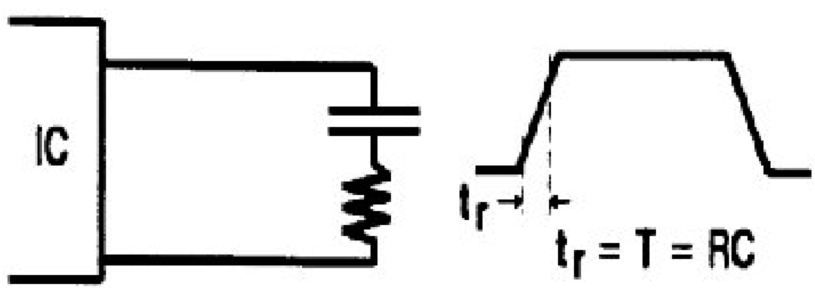

Figure 13-4 Exponential Wave Shaping

Wave shaping can be accomplished on line drivers with no built-in wave shaping capability by applying controls to the drivers output, or, in the case of Op-amp type drivers, by adding feedback to bandwidth limit. The wave shaping circuitry added to a standard line driver is similar to the RC control mentioned above with either dissipative (RL) or reflective (LC) designs. The added circuitry is placed between the driver's output and the transmission line, and is considered as a part of the driver's output impedance.

Some interfaces, such as edge triggered receivers, require special wave shaping. For edge triggered devices, it is important not to round off the signal beyond the maximum signal rise time required by the receiver. Notice in Figure 8.5 that even a slight change in signal rise time can drastically effect the real time of occurrence when the minimum turn on voltage for the device to switch states is reached.

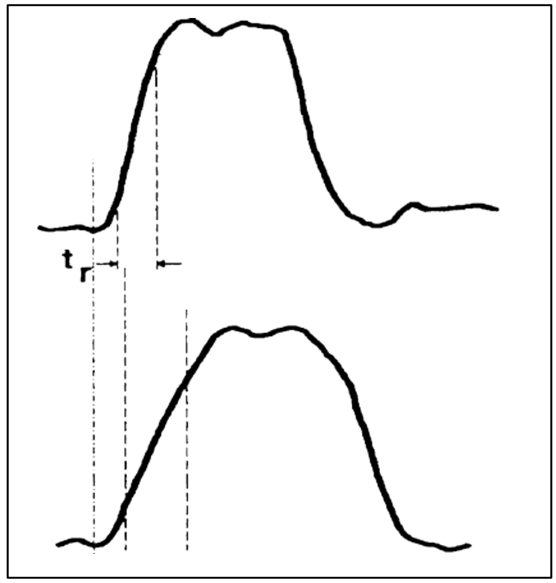

Figure 13-5 Drastic Rise Time Changes Can Occur

Line Receiver Characteristics

A line receiver has five primary characteristics of interest to system designers: input impedance, sensitivity, hysteresis, and input threshold. Designing a line receiver for the first of these characteristics, input impedance, is fundamental to the reduction of reflected signal noise. Figure 13-6 shows a transmission line with characteristic impedance $z_{(0)}$ and a line receiver with an input impedance of $Z_L = R_L$.

As previously described, if the load and characteristic impedance are not equal, power incident on the line receiver will be reflected. In most cases, the designer is required to match the characteristic impedance of the line with additional impedance which satisfies the equation below:

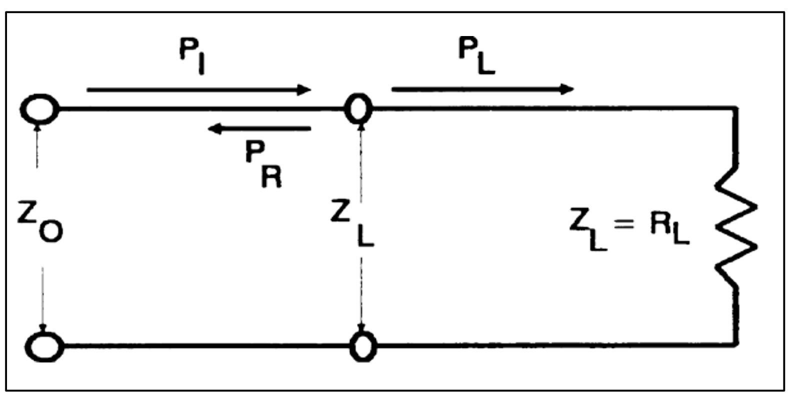

Figure 13-6 Transmission Line Model

$$Z_{(L)} = \frac{Z_{(R)} Z_{(T)}}{Z_{(R)} + Z_{(T)}}$$

$Z_{(L)}$ is the load impedance and $Z_{(R)}$ is the line receiver impedance in parallel with the terminating impedance $Z_{(T)}$ from Figure 13-6. Therefore, to design or upgrade a line receiver so that it has no reflected power, a terminating impedance is required which satisfies the equation $Z_{(L)} = z_{(0)}$, or:

$$Z_{(T)} = \frac{z_{(0)} Z_{(R)}}{Z_{(R)} - z_{(0)}}$$

A line receiver's sensitivity and hysteresis can be found in the manufacturer's published data. Hysteresis generally provides noise immunity of several tenths of a volt for single ended systems. It can also be the source of ringing on the transmission line. Some line receivers have an externally controllable voltage input switching threshold. The Texas Instrument SN7514O dual line receiver has a reference voltage pin for each receiver which allows the designer to specify the input switching threshold, as shown in the function table of Table 1. The reference voltage can be varied between 1.5 volts and 3.5 volts.

Table 1

Line Input	Strobe	Output
-100 mV	L	H
V reference		
+100 mV	X	L
X	H	L
SN7514O LINE RECEIVER		

Transmission Line Examples

The schematic of a typical line driver (SN75188) was shown in Figure 13-7. This line driver's curve of output current versus voltage in shown in Figure 13-8. To simulate a typical TEMPEST system application, a short interface cable was attached between the driver and its intended receiver interface circuit. When radiated emission measurements were made, significant signal related emissions were detected radiating directly from the interface cable.

Upon closer examination of the line driver's hysteresis curve, a small three volt change can be noted during the time when current reverses direction. The effect of this voltage change in a TEMPEST controlled system environment was to cause ringing along the transmission line resulting in radiated emissions.

Two "fixes" are possible to correct the short cable radiation problem while still maintaining the output waveform within a typical secure system's specified performance requirements.

Basically, the intent is to maintain a smooth voltage transition during the time when current changes direction.

Figure 13-9 shows the desired fixes to reduce the TEMPEST emission problem. First, a capacitor can be added between the driver output and the -Vcc pin to reduce the effect of the hysteresis notch. Since this change also changes the output waveform, an inductor is placed in series on the transmission line to restore the signal waveform's shape. The capacitor thus became the energy source for the output signal during the transition period.

The second capacitor can be added to load the interface cable, reduce the effects of inductive reactance from the inductor, and better match output impedance to the short cable. Notice in the figure that this capacitor is returned to the signal reference ground of the driver. The combination of the two fixes will effectively eliminate the previous emission problem.

For simple zero to plus level outputs, if the output data rate is low enough, and if a more significant board level fix can be justified, the same wave shaping effect

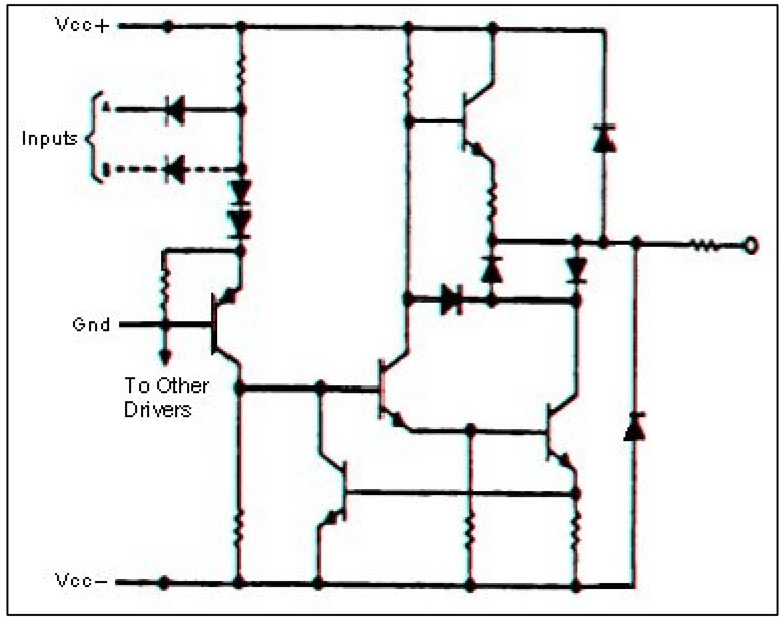

Figure 13-7 Schematic of a Typical Line Driver (SN75188)

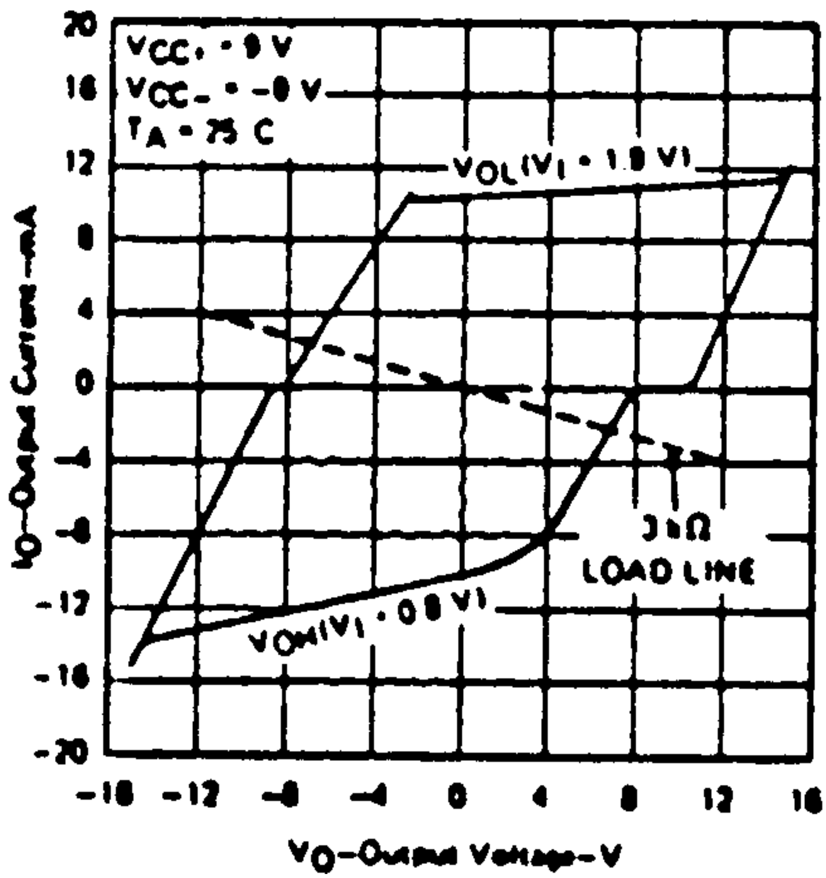

Figure 13-8 Hysteresis Curve

can be achieved by removing the entire line driver and using a three terminal voltage regulator as the driver circuit.

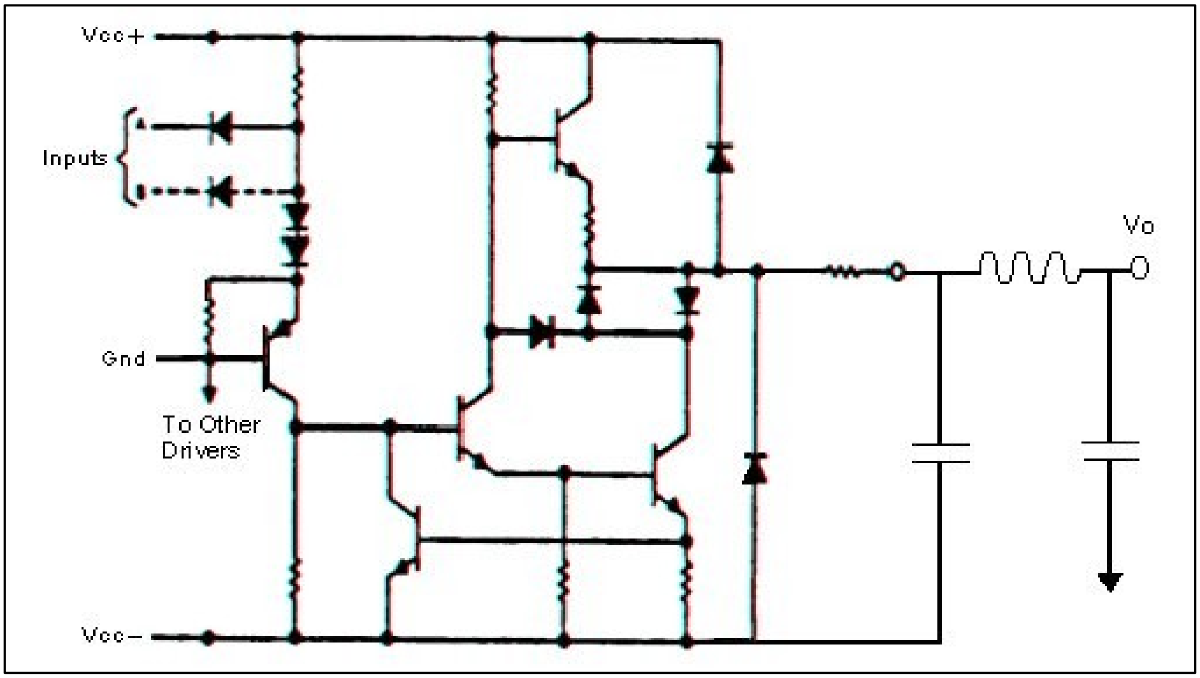

Figure 13- 9 Modified Line Driver Fixes

In another example, the unfiltered output of a Motorola 1488 line driver, used for RS-232 applications, produces a noisy square wave output. Often, the high frequency components of this square wave output are mismatched to the transmission line impedance, resulting in significant radiated noise above the specified emission limits.

As a solution to this problem (Figure 13-10), the output signal can be wave shaped to reduce the radiated noise by placing a circuit card type filter between the line driver and the short shielded output wire inside the box containing the driver. Since off the shelf filters normally are grounded to case, and since there is normally significant inductance in a typical unit's ground system between the chassis and the driver return, the card type filter should be mounted immediately adjacent to the circuit card containing the driver in order to prevent a chassis ground loop. On the box wall itself, a pin filtered ferrite type connector can then be used to reduce any high frequency signals which might have inadvertently coupled through the shield to the internal signal line wire inside the box. Again, it is most important to stress that component type filter circuits must be carefully evaluated concerning where they shunt noise current.

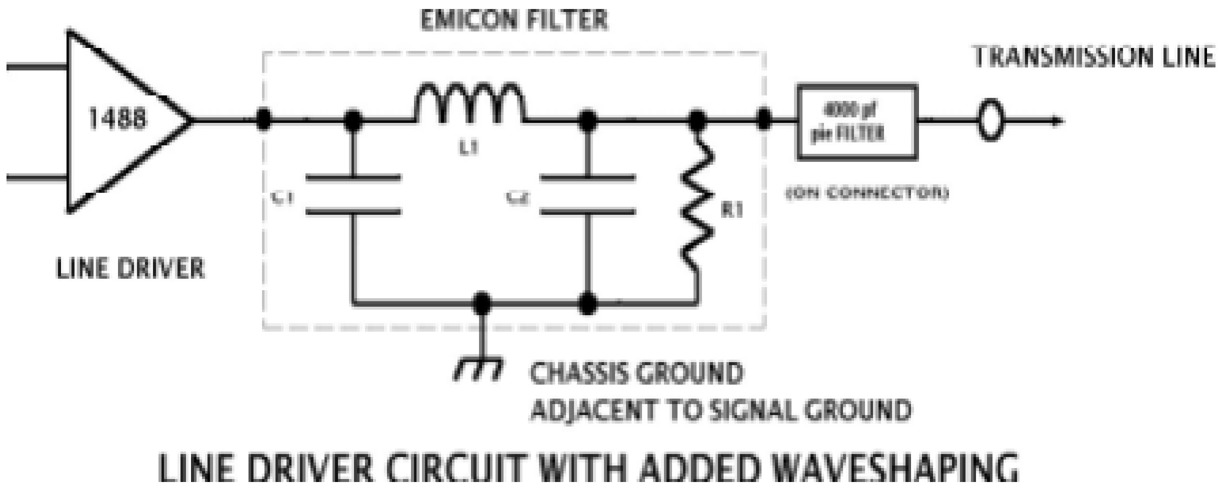

Figure 13-10 1488 Line Driver Modification

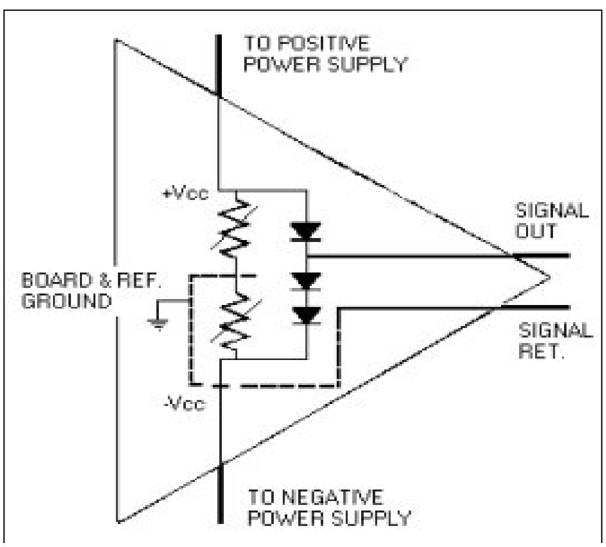

Figure 13-11 Equivalent Bias in OpAmp

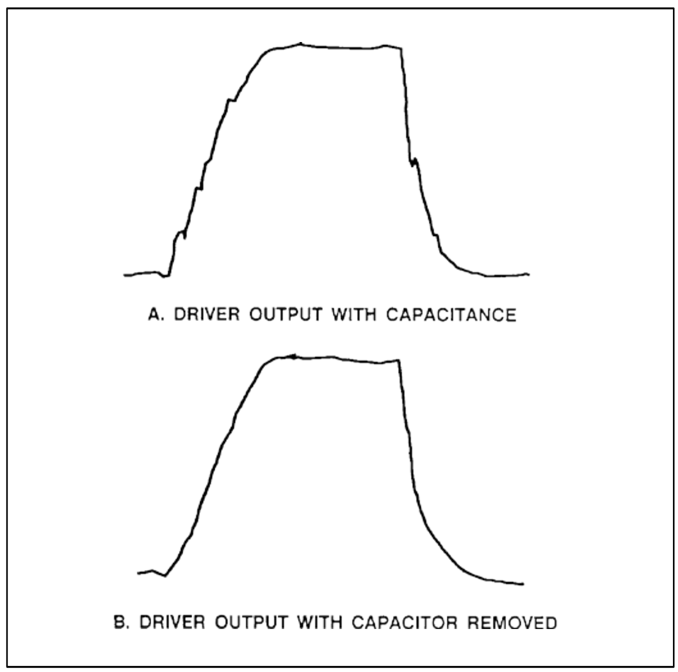

Figure 13-12 Wave Shape with Design Modification

Line Driver Bias Equivalent

Figure 13-11 shows the internal equivalent design of a typical OpAmp driver. The result of internal coupling is the equivalent biased driver circuit driving a low level signal source into the ground system. This signal appears as a low level common mode voltage on all other boxes referenced to the same ground platform.

In difficult to control cases, the output of the driver in Figure 13-10 could look like Figure 13-12A. Notice in this case that small voltage spikes might still be present on the waveform. To correct this problem, remove C1 from the commercial filter. This modification has the effect of increasing the impedance at high frequency to the line driver, and results in the waveform shown in Figure 13-12B.

The third example, Figure 13-13, shows bandwidth limiting used with an OpAmp driver circuit. In this case, the driver is used on a Black digital output line. OpAmp powerline rejection is not a problem for the example with the use of controlled power, such as RC, LC, or ferrite decoupling to the OpAmp power inputs. However, since there is a potential for high frequency signals to be coupled to the OpAmp's signal input leads, also reducing the operational bandwidth of the device effectively eliminates the majority of signal input coupling problems.

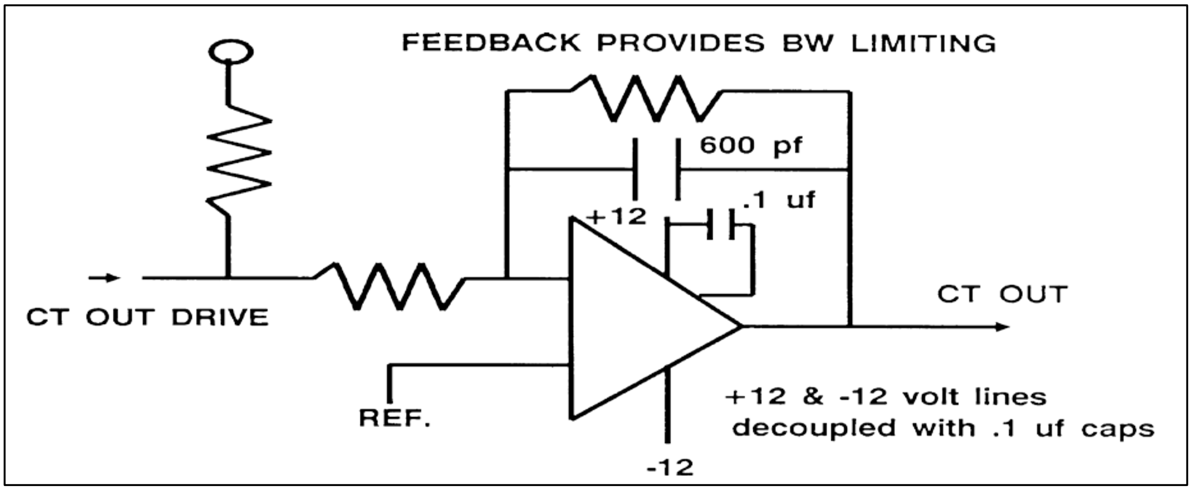

Figure 13-13 Bandwidth Limiting an OpAmp

Figure 13-14 is a practical fix for the Motorola MC 1489P line receiver. In this example, a peripheral device receives Red data from a line driver located inside an existing TEMPEST pc. Since users must access the peripheral through the already secure pc, emission security of the network is localized only to the pc/peripheral device interface.

A security problem could result in this case only if internally coupled signals escape from within the peripheral device through radiation or ground loop conduction. For the condition where an existing line receiver is already designed and located inside the peripheral device, the thrust of a control effort could be to locate the peripheral in a less sensitive (more emission secure) area, or to add on board fixes at the line receiver device. In the case of the MC 1489 P, one set of fixes that effectively suppress internal generated signals are to provide additional decoupling through the inductor/capacitor circuits shown, increase the resistance and capacitive values near the RS-232 connector, and add ferrites to reduce high frequency harmonics on the signal lines.

Figure 13-15 is the suggested MIL-STD 188C wave shaper-driver design using discrete transistors.

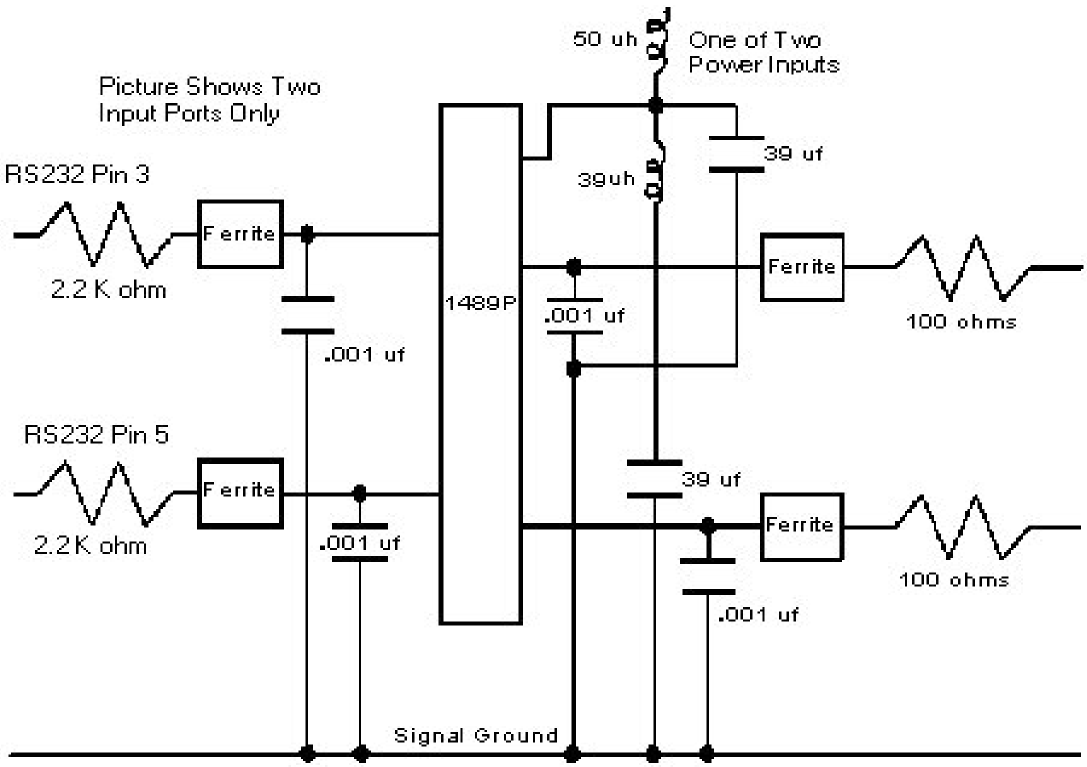

Figure 13-14 Modified MC1489P Line Driver

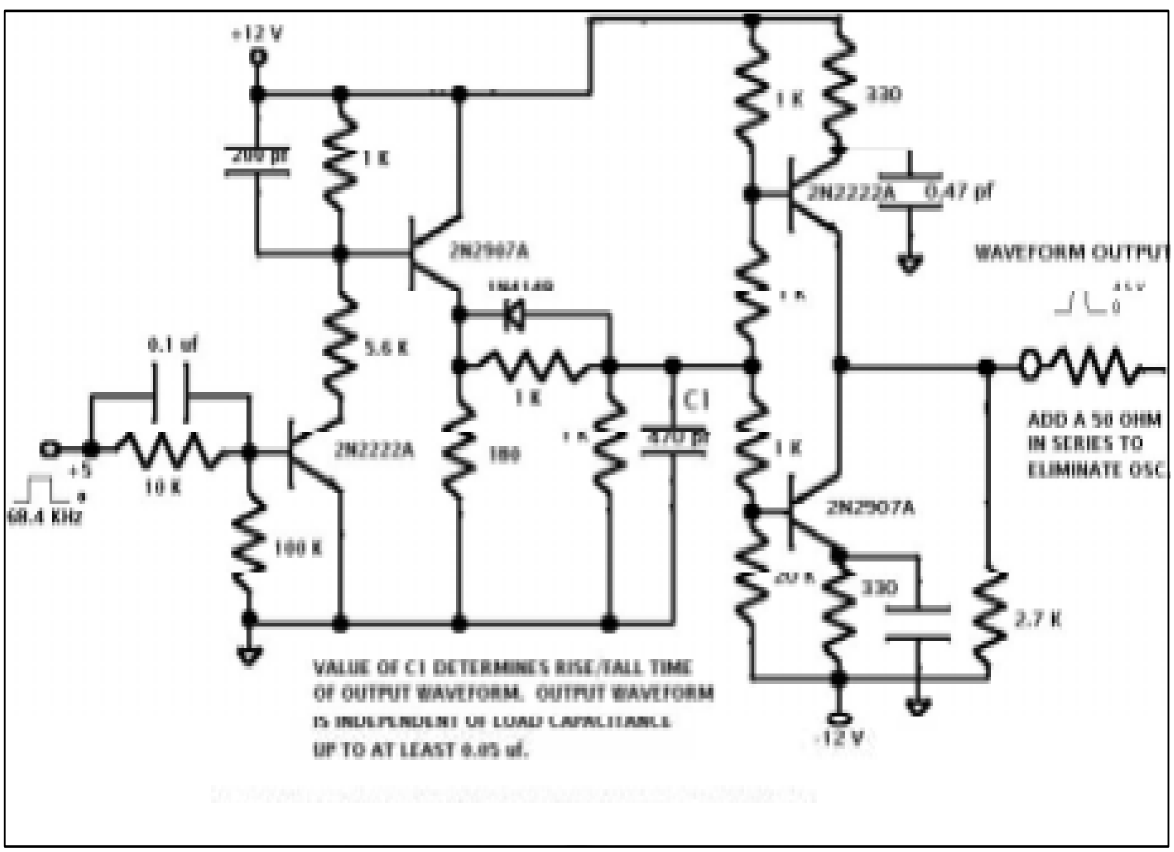

Figure 13-15 MIL-STD 188C Wave Shaper/Driver

The standard MIL-STD 188C wave shaper/driver circuit has a problem in that when inductively loaded by a transmission line, the combined effects of the inductance and the internal coupling capacitance of the 2N2222A transistor effectively turn the driver into a Colpitts oscillator. As was shown in Figure 13-15, by adding a 50 ohm resistor in series with the output, the increased damping eliminates the oscillator effect.

Line Receiver Characteristics

The primary characteristics of a line receiver are input impedance, sensitivity, hysteresis, and input threshold. Designing a line receiver for the first of these characteristics, input impedance, is fundamental to the reduction of reflected signal noise. Decoupling is the primary means of reducing crosstalk and noise. The solution to decoupling problems is to provide differential and common mode decoupling for the critical interface lines as near to the device as possible. Differential decoupling should be accomplished using capacitors of very low inductance with loading appropriate for the switching frequencies required. Figure 13-16 shows a simple protected differential line receiver that also provides protection from lightning, EMP, and noise problems.

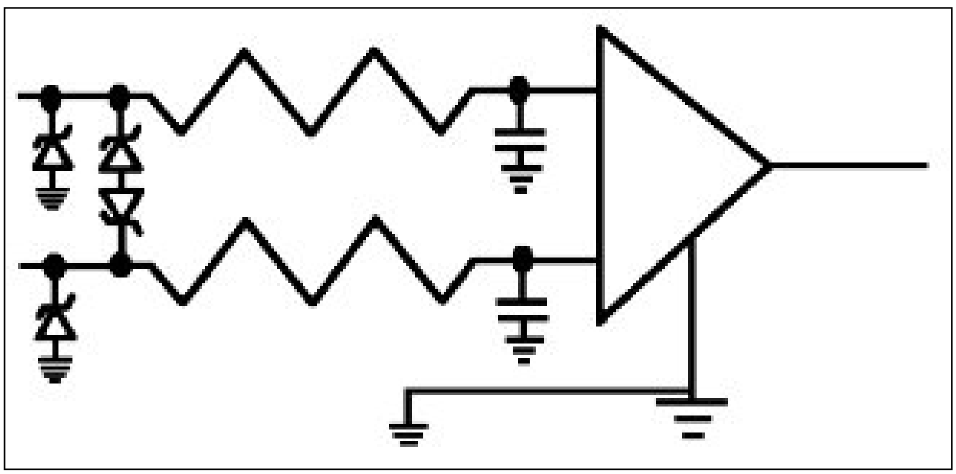

Figure 13-16 Protected Differential Line Receiver

Fiber Optics

Susceptibility and emission coupling problems in line drivers and receivers are often overcome using fiber optic cables. In these cases, electrical ground loops are eliminated between communications equipment and between separate power systems. Fiber optic line drivers require current levels that can themselves generate strong emissions. Unfortunately, these driver generated emissions are difficult to suppress. In full duplex operation, crosstalk isolation may also be defeated by physical light coupling on the board. LEDs on visible signal emitters are fast enough to re-generate true data impulses.

IC DIP Type Filters

A number of organizations supply DIP type IC filters, such as the configuration shown in Figure 13-17, to help control buss and multi-wire interface signal emanations. The filters act to:

1. Reduce the emission of intelligence bearing noise by filtering out the high-frequency content of digital signals at the board level.

2. Replace the expensive and bulky inductive devices typically used to suppress conducted emanations.

3. Minimize space and routing problems, and reduce manufacturing cost per installed resistive and capacitive function.

4. Increase board yields and reliability by reducing component count.

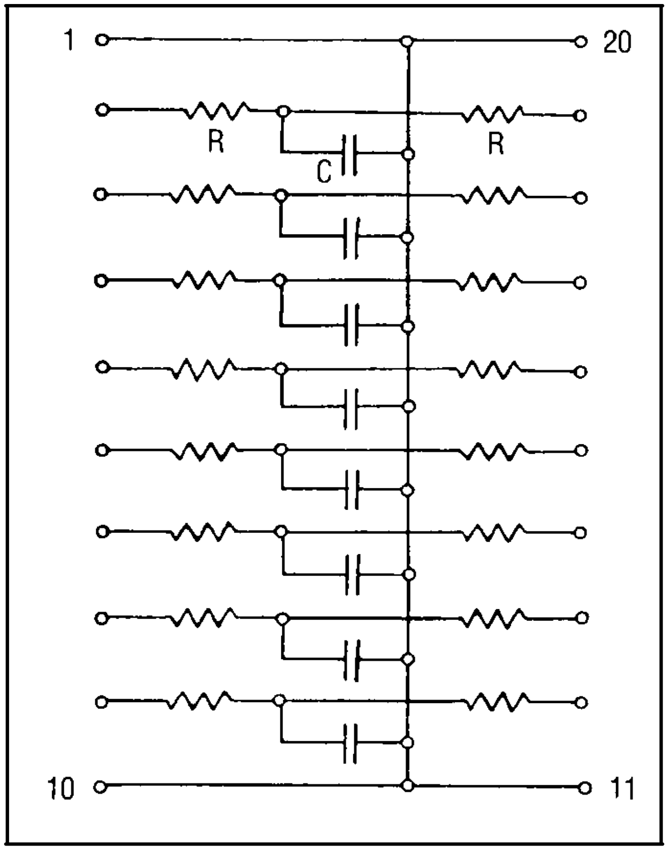

Figure 13-17 Typical DIP Type RC Filter Package

While several approaches are available at the board level to control emissions, including grounded metal enclosures, shielded cables, judicious component placement and interconnect designs, and power-supply decoupling, low- pass filtering is particularly effective when the noise components to be rejected occur at frequencies higher than the signal frequency (to be passed). For these situations, low-pass resistor-capacitor filter networks are ideal.

A typical application would be to filter signal lines between RS-232 drivers and their corresponding connectors. In such low to medium frequency applications, these networks represent a more useful (and economical) solution than inductive type filters such as ferrite beads. In fact, ferrite beads become mostly ineffective below 1OMHz. Notice the typical response curves for RC type filters shown in Figure 13-18[2].

The basic "T" configuration (Figure 13-17) is a standard R-C network normally available in versions for 7 or 8 input signal lines. Under steady state conditions, the capacitor C offers infinite impedance to the DC component of the input waveform. Thus, the DC component of the signal voltage is passed to the load, but reduced in value by the voltage drop across the two resistors.

[2] Guide to Network Applications: EMI/RFI Filtering, Bourns Networks, Inc., Riverside, CA, 1990.

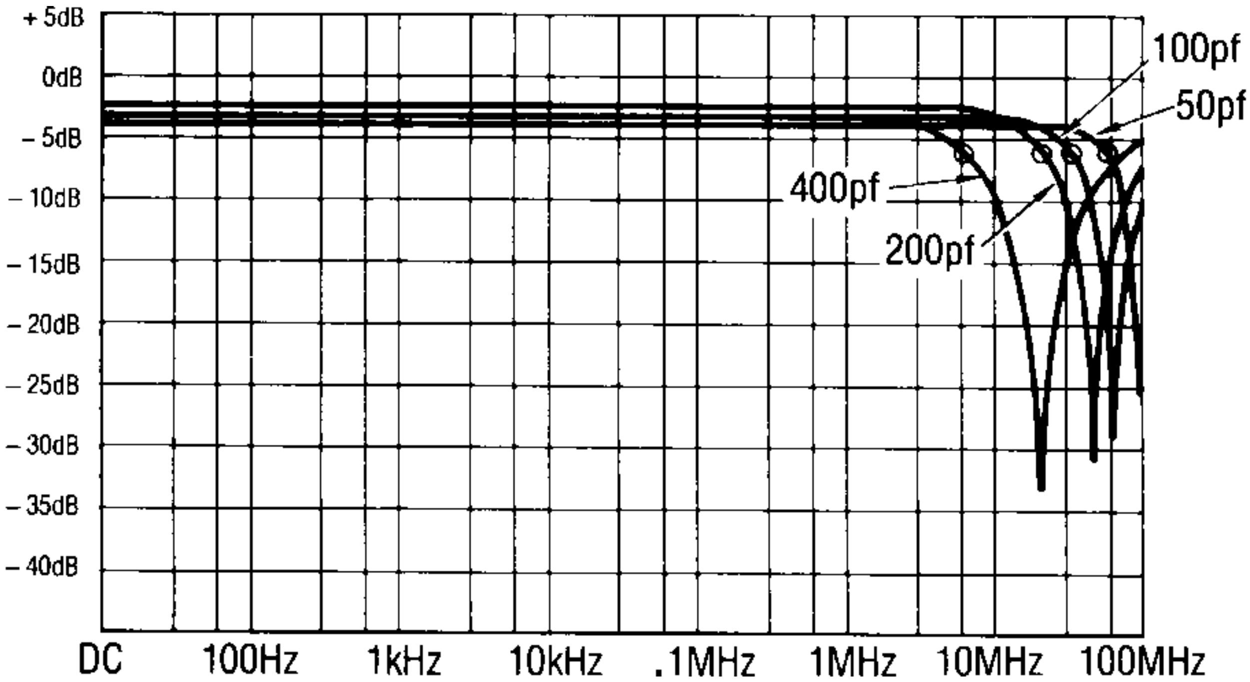

Figure 13-18 Typical Response Curves

The impedance of C becomes lower at higher (noise) frequencies. Therefore, the noise component of the signal faces a voltage divider consisting of the first resistor (R) and C. At the high frequencies of the noise component, R will be much greater than the impedance of C. Most of the noise voltage will be dropped across the resistor. Almost no noise current flows through the load, and, therefore, will hardly affect the DC voltages (i.e., the signal) across the load.

Since the filter is symmetric, its principle of operation is the same for waveforms traveling in the opposite direction, in which case the voltage divider is formed by the second resistor and the capacitor. Such a symmetrical design is useful for filtering signals on a bidirectional bus.

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{j\omega C\,(R + R_S)(R + R_L) + (R_S + R_L + 2R)}$$

Assuming purely resistive source and load impedances, the transfer function is given by: RL is the load resistance and RS is the source resistance of the filter.

RC Filter Component Selection

The "roll-off" frequency fc, defined as the frequency at which the filter passes one-half the power it receives at its input terminal, is normally specified from the low megahertz range up to about 100 MHz. This frequency, also known as the "-3 dB" frequency, is determined by the R and C values chosen, and should be selected to attenuate at frequencies no lower than harmonics above the third harmonic of the intended signal to be transmitted.

The specification of these values will depend on constraints relating to problem frequencies being conducted, system performance, driver loading, and available products or components. The following procedure is suggested to choose appropriate values of R and C.

The first step is to determine the desired roll-off frequency of the filter, which will lie between the signal frequency and the dominant frequencies of the problem noise. By determining the pole of the filter (setting the denominator of the transfer function equal to zero), the roll-off frequency can be expressed in terms of R and C:

$$f_c = \frac{R_S + R_L + 2R}{2\pi C\,(R + R_S)(R + R_L)}$$

R_L is again the load resistance, and RS is the source resistance of the T-filter.

Remember, the RC combination must be chosen so that the additional RC time delay will not result in exceeding the sampling window of the receiving IC, due to excessive lengthening of signal rise and fall times. Rise time from 10% to 90% of the waveform amplitude can be calculated in terms of the circuit's RC time constant using the 1 - exp (-t/RC) relationship for a charging capacitor. At 10%, t_L = 0.1 time constants, and at 90%, t_H = 2.3 time constants. "Time constant" equals $R_{th}C$, where R_{th} is the Thevenin-equivalent resistance as seen by the capacitor.

Equating the difference in the two time constants to the maximum tolerable rise (or fall) time:

$$t_{\max} = t_H - t_L = 2.2\ R_{th} C$$

$$t_{\max} = 2.2\,\frac{(R + R_S)(R + R_L)}{R_S + R_L + 2R}\,C$$

A final consideration is the insertion loss. As mentioned previously, the voltage drop across the two resistors will attenuate the voltage reaching the load. Normally, logic high and low levels should still be within valid limits of gate operation. Although signal attenuation can be minimized by choosing small R values relative to the load impedance, for enhanced security, signal attenuation must sometimes be maximized to the extent tolerable. Typical values for R range from 10 to 50 ohms.

In The Final Analysis

The equipment interface circuit consists of a line driver and its external circuitry, the transmission line, and the line receiver and its external circuitry. The choice of each component is dependent upon the required interface standard and the noise environment the circuit is exposed to. The choice of each component is also dependent on the data rate to be transmitted, the length of the transmission line, and on the sensitivity of the receiving circuitry. In all cases, it is best to judiciously design the entire interface specifically for its intended application.

Bibliography

1. B.C. Gabrielson, The Aerospace Engineers Handbook of Lightning Protection, ICT Publishing, Gainesville, VA, 1988.

2. D.K. Cheng, Field and Wave Electromagnetics, Addison-Wesley, Reading, MA, 1983.

3. EIA Standard RS-423-A, Electrical Characteristics of Unbalanced Volt age Digital Interface Circuits, December 1981.

4. B.C. Gabrielson, TEMPEST, A Description and Application, ITEM Magazine, R & B Enterprises, 1984.

5. B.C. Gabrielson, Interfacing For Quieter Transmission Lines, AFCEA, 1989.

6. R.L. Walter IV, Specifying and Designing Equipment Interface Circuitry Which Meets EMC/EMI Requirements, EMC EXPO 88, Washington D.C.